AMENDMENTS TO THE CLAIMS

Claim 1 (Original) A transmission path latency measurement method which measures a latency on a digital transmission path between a first data transmission device and a second data transmission device interfacing to each other by using three or more kinds of signal patterns, the transmission path latency measurement method comprising:

when a first signal pattern is detected among received signals, modifying a transmitting signal to a second signal pattern;

when the second signal pattern is detected among the received signals, modifying a transmitting signal to a third signal pattern;

when a signal pattern is detected among the received signals, modifying a signal pattern of a transmitting signal;

when a last signal pattern is detected among the received signals, modifying a transmitting signal to the first signal pattern;

when any one of the signal patterns is not detected among the received signals or when two or more signal patterns are synchronously detected among the signal patterns, transmitting and receiving a signal between the first data transmission device and the second data transmission device so as to maintain a signal pattern of a transmitting signal existing immediately before; and

measuring a time between the moment when the first signal pattern is transmitted and the moment when the second signal pattern is detected, a time between the moment when the second signal pattern is transmitted and the moment when the third signal pattern is detected, a time between the moment when the signal pattern is transmitted and the moment when the signal pattern is detected, and a time between the moment when a last signal pattern is transmitted and the moment when the first signal pattern is detected as a latency between the transmission paths.

Claim 2 (Original) The transmission path latency measurement method according to claim 1, wherein a plurality of signal patterns are pseudo random patterns.

Claim 3 (Original) A transmission path latency measurement device comprising:

a transmission timing pulse output unit which outputs a transmission timing pulse;

a first signal pattern output unit which generates and outputs a first signal pattern in accordance with an input of the transmission timing pulse;

a third signal pattern output unit which generates and outputs a second signal pattern in accordance with an input of the transmission timing pulse;

an output signal pattern output unit which generates and outputs a signal pattern in accordance with an input of the sequential transmission timing pulse;

a last signal pattern output unit which generates and outputs a last signal pattern in accordance with an input of the transmission timing pulse;

a transmitting signal output unit which selects any one of the first signal pattern to the last signal pattern input by the first signal pattern output unit to the last signal pattern output unit and outputs the selected signal pattern as a transmitting signal;

first to last signal pattern detection units which output a detection signal when the first signal pattern to the last signal pattern are detected among the received signals;

an output signal selection unit which outputs a selection signal with respect to the transmitting signal output unit in accordance with the detection signal input from the first to last signal pattern detection units; and

a transmission path latency calculation unit which calculates a transmission path latency by using the transmission timing pulse and the selection signal,

wherein the output signal selection unit outputs the selection signal with respect to the transmitting signal output unit such that the transmitting signal is modified to the second signal pattern when only the first signal pattern is received as the received signal, outputs sequentially the selection signal with respect to the transmitting signal output unit such that the transmitting signal is modified to the third signal pattern when only the second signal pattern is received as the received signal, and outputs the selection signal with respect to the transmitting signal output unit such that the transmitting signal is modified to the first signal pattern when only the last signal pattern is received as the received signal.

Claim 4 (Original) The transmission path latency measurement device according to claim 3, wherein the transmission path latency calculation unit determines sequentially a transmission starting time of the first signal pattern, a transmission starting time of the

second signal pattern, and a transmission starting time of the last signal pattern, calculates a difference between the transmission starting time of the first signal pattern and a detection starting time of the second signal pattern, a difference between the transmission starting time of the second signal pattern and a detection starting time of the third signal pattern, and a difference between the transmission starting time of the last signal pattern and a detection starting time of the first signal pattern as a transmission path latency, and subtracts (the number of bits necessary for signal pattern detection) × (interval of transmission timing pulse) × 2 , as a correction value, from the transmission path latency in accordance with a requested value.

Claim 5 (Currently Amended) The transmission path latency measurement device according to claim 3 ~~or 4~~, wherein the three or more signal patterns are pseudo random patterns.

Claim 6 (Original) The transmission path latency measurement device according to claim 5, wherein the signal pattern output units for the first signal pattern, and the second signal pattern through the last signal pattern, and the signal pattern detection units for the first signal pattern and the second signal pattern through the last signal pattern include a shift register and an exclusive OR logic circuit.

Claim 7 (Currently Amended) A data transmission device comprising the transmission path latency measurement device according to claim 3 ~~any one of claims 3 to 6~~ as a transmission path latency measurement unit.

Claim 8 (Currently Amended) A semiconductor chip comprising the transmission path latency measurement device according to ~~any one of claims 3 to 6~~ claim 3.

Claim 9 (Currently Amended) A method of detecting the formation of a loop on a transmission path by using the transmission path latency measurement method according to claim 1 ~~or 2~~, the method comprising:

selecting at least one signal pattern among the first signal pattern to the last signal pattern; and

determining that with respect to the selected signal pattern a loop is formed on the transmission path when a phase difference between a transmission starting time when the selected signal pattern is selected as a transmitting signal and a time when a signal pattern is detected from the received signal is included in a predetermined range.

Claim 10 (Original) The method of detecting the formation of a loop on a transmission path according to claim 9, wherein the selected signal pattern are a pseudo random pattern.

Claim 11 (Currently Amended) A device for detecting the formation of a loop on a transmission path by using the transmission path latency measurement method according to claim 1 ~~or 2~~, wherein at least one signal pattern is selected among the first signal pattern through the last signal pattern, and when with respect to the selected signal pattern a phase difference between a transmission starting time at which the selected signal pattern is selected as a transmitting signal and a time at which a signal pattern is detected from the received signal is included in a predetermined range, it is determined that a loop is formed on the transmission path.

Claim 12 (Original) The device for detecting the formation of a loop on a transmission path according to claim 11, wherein the plurality of signal patterns are pseudo random patterns.

Claim 13 (Currently Amended) A data transmission device comprising the device for detecting the formation of a loop on a transmission path according to claim 11 ~~or 12~~ as a unit for detecting the formation of a loop on a transmission path.

Claim 14 (Currently Amended) A semiconductor chip comprising the device for detecting the formation of a loop on a transmission path according to claim 11 ~~or 12~~.

Claim 15 (New) The transmission path latency measurement device according to claim 4, wherein the three or more signal patterns are pseudo random patterns.

Claim 16 (New) The transmission path latency measurement device according to claim 15, wherein the signal pattern output units for the first signal pattern, and the second signal pattern through the last signal pattern, and the signal pattern detection units for the first signal pattern and the second signal pattern through the last signal pattern include a shift register and an exclusive OR logic circuit.

Claim 17 (New) A data transmission device comprising the transmission path latency measurement device according to claim 4 as a transmission path latency measurement unit.

Claim 18 (New) A data transmission device comprising the transmission path latency measurement device according to claim 5 as a transmission path latency measurement unit.

Claim 19 (New) A data transmission device comprising the transmission path latency measurement device according to claim 6 as a transmission path latency measurement unit.

Claim 20 (New) A semiconductor chip comprising the transmission path latency measurement device according to claim 4.